



SHAPING THE NEXT GENERATION OF ELECTRONICS

JUNE 23-27, 2024

MOSCONE WEST CENTER
SAN FRANCISCO, CA, USA



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Die, Package and PCB Co-design for low Area, high Signal to Power pin ratio in High Frequency SOC designs

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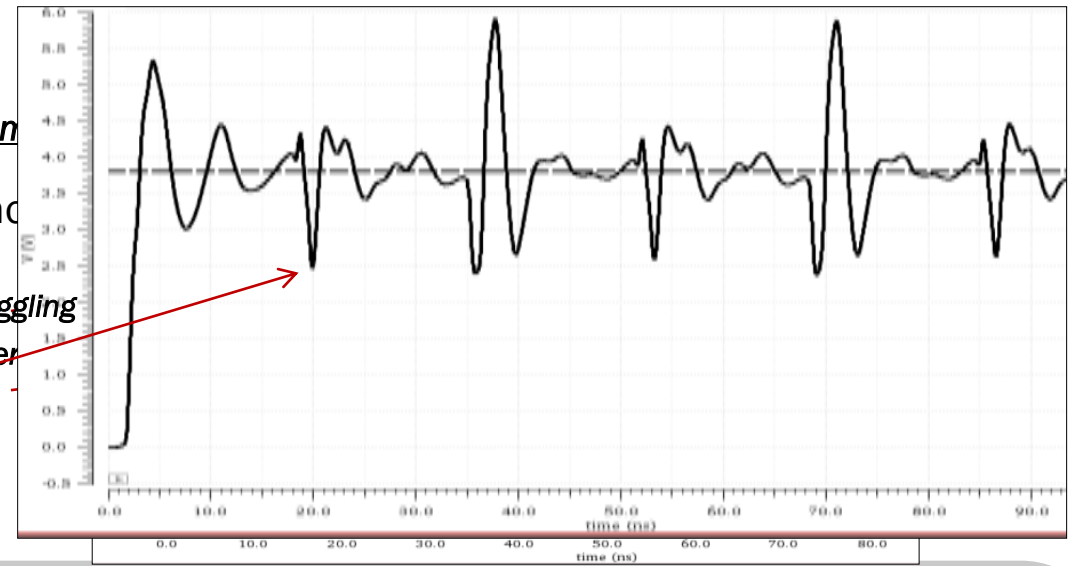
Outline

- Signal Integrity and SSN
- Motivation/Problem Statement
- Pictorial Representation through flow chart
- Solutions walk-through
- Proposed Solution summary
- Results and Summary

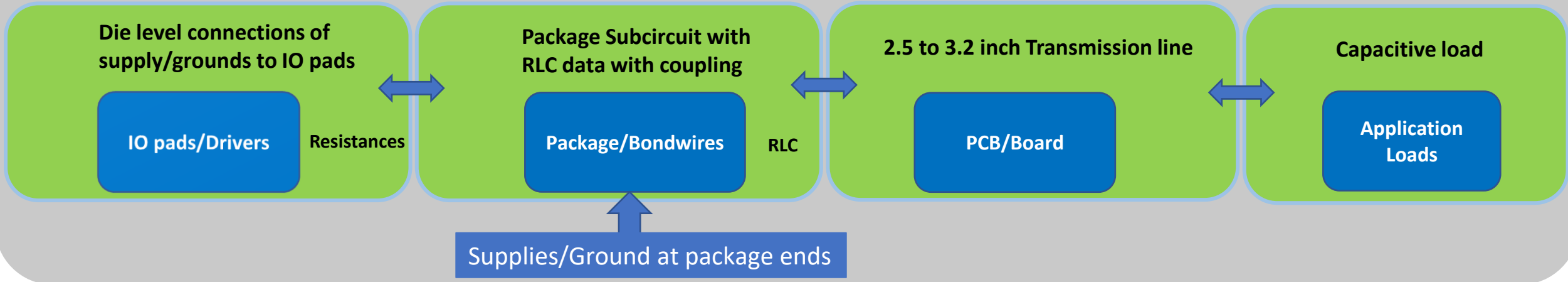
Signal Integrity

- Understanding Signal Integrity
- Simultaneous Switching Noise (SSN)
- Influencing Factors of SSN

All pads in same state
Overshoot
One Pad Static 1 and other pads toggling
One Pad Static 0 and other pads toggling
VIL
QLN-Static 1



Representation of SSN

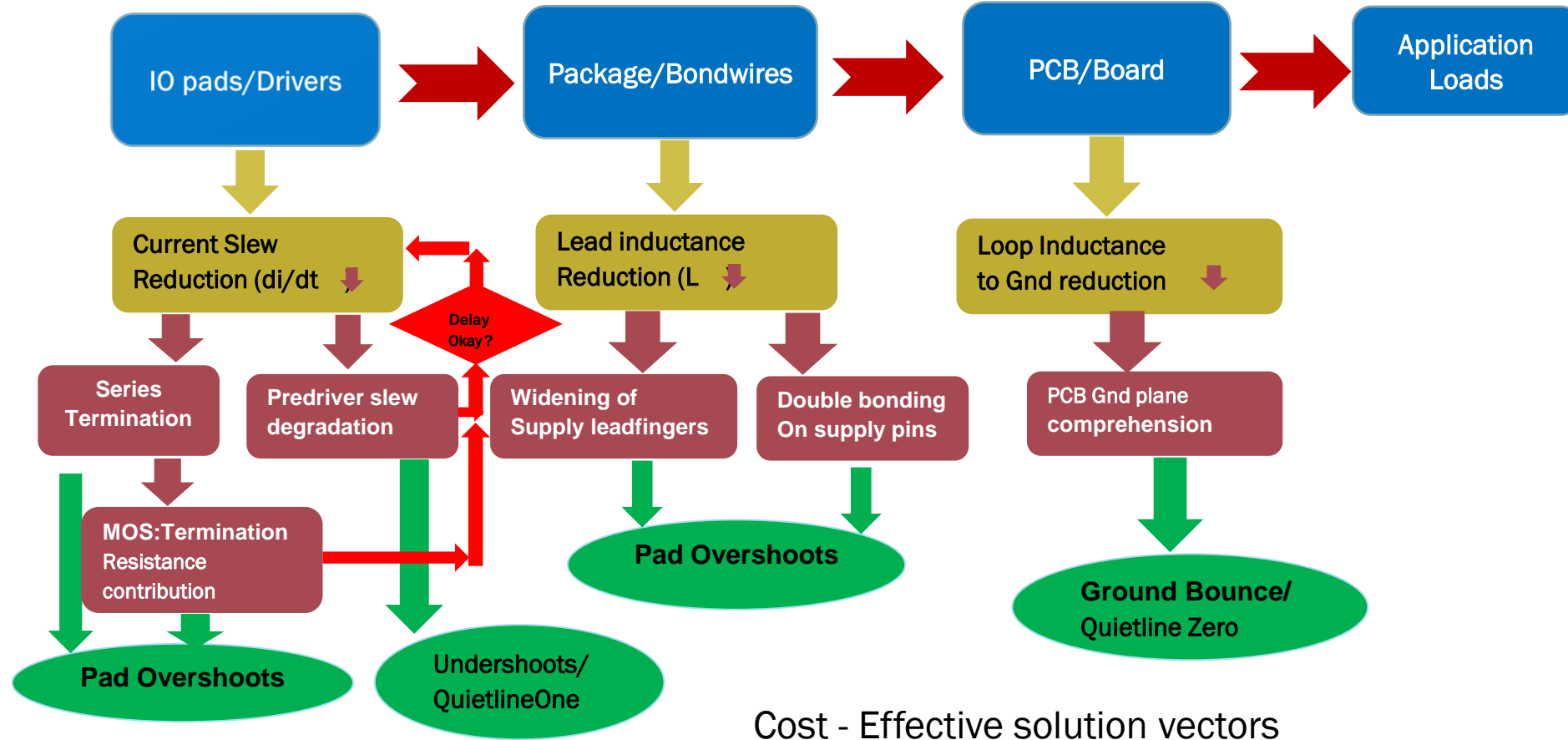


Signal Integrity (SI) on IO pads is measured wrt aspects like pad-overshoots, ground-bounces, undershoots. These are typically measured where transistors exhibit faster slew in signals i.e, strong process, low temp, higher voltages.

Motivation/Problem Statement

- Microcontroller competitive targets – More signal output pins from chip with minimal power, ground pins.
- New Targets in design :
 - Power-pins reduction by 40% on Core and IO power supplies, thereby providing more pins for GPIOs.
 - Increase in supply tolerance. 5% to 10%.
- These two targets have negative impacts on IR drop, timing, Signal Integrity (SI), and hence overall design performance.
- When supply pins get reduced, there would be more di/dt on available supplies plus additional GPIOs add more current – resulting in much higher surge of current per supply.
- Usage of existing IO pads have degraded SI aspects by big margins due to Ldi/dt on supply pins.
- Reduce drive strength of IO pads to reduce the current di/dt ?
- Industrial solutions like PTV compensation circuits, programmable drive cells ?
- Through this paper we present cost-effective (area) design strategies that were incorporated to keep all the above design vectors in reasonable limits **without area penalties**. We will showcase the signal-integrity aspects wrt GPIO pads and see how they were addressed.

Solution Vectors



Fixes at

Die : IO pads, Driver and Predriver Improvements

Package : Bondwire or Leadfinger parasitics reduction

PCB : Comprehension of PCB plane for complete

Solutions and Results

- IO Pad Improvements : Dealing with di/dt
- Series Termination (R_s)/MOS: R_s ratio : Series termination which reduces drive is used to control overshoots. However, heavy usage of R_s would make the IO pad's incapable of driving higher performance loads, hence a better balance is drawn b/w MOS and R_s factor, along with some margin so that other optimizations don't bring the drive below minimum requirements.
- Predriver degradation : Faster slews on pads and also multiple signal transitions together would multiply signal degradation. Driver cannot be reduced due to minimum drive requirements, hence predriver degraded to reduce transition slews – helped reduce pad overshoot by some factor.

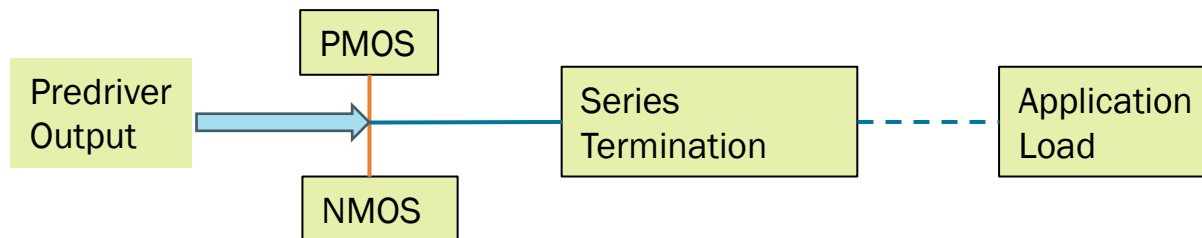


Fig. Series Termination

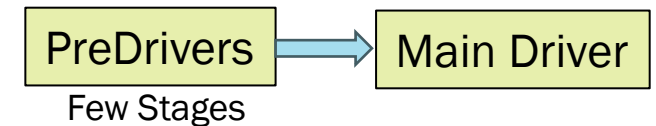
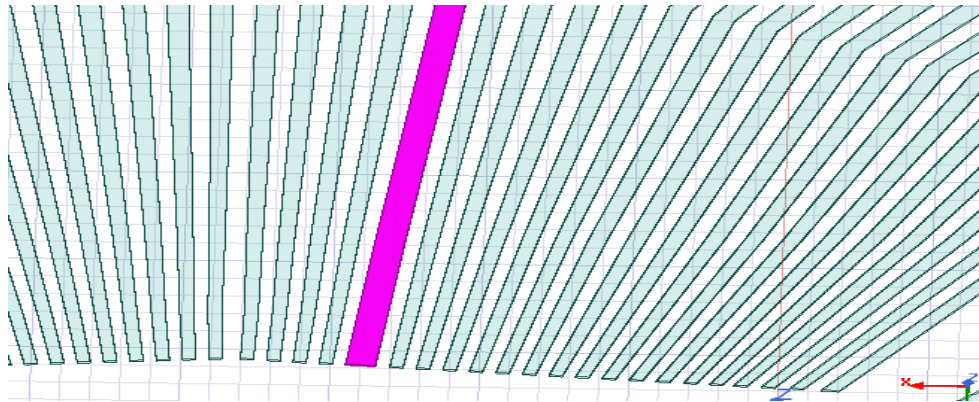


Fig. IO Output stage

Solutions and Results

Leadframe Enhancements, Double-bonding : Dealing with inductance L

- Widening, Increasing thickness : All package leads have almost equal width. To reduce supply pin inductance, respective lead has been widened.
- Thickness can also be increased, however, it has new tooling requirements, plus might increase coupling, didn't pursue, but an option.
- Double bonding : Adding another bondwire in parallel to existing supply wire reduced inductance further.



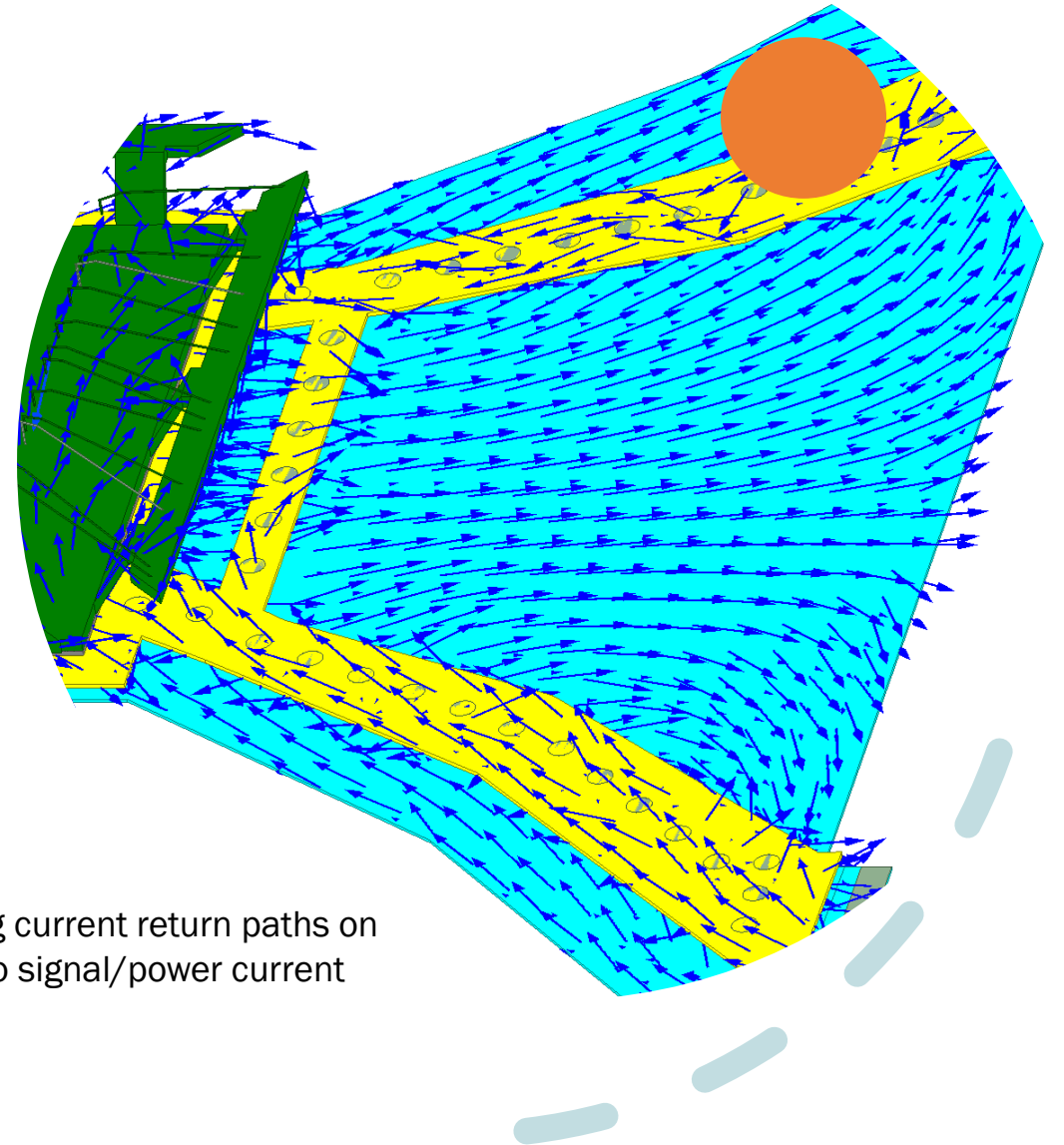
Wider Lead
for supply pin

Fig. Leadfingers of the package

Above two factors have helped in reduction of pad-overshoots and undershoots. Ground bounce was still above limits – where PCB Gnd comprehension helped.

Solutions and Results

- PCB Gnd : Generic practice on PCB from SI perspective is to provide a closer loop between supplies to ground or signals to ground – to reduce loop inductance (L_{sg} – loop ind. Supply, ground)
- Providing grounds next to supplies in package is not possible always due to pin count aspects.
- Hence, PCB level solution, Ground plane has been extended to cover signal leads, power-leads
 - which reduced L_{sg} and helped to reduce ground bounce by significant amount.



Representative picture showing current return paths on yellow PCB plane as opposite to signal/power current

Summary of Solutions

Solution that we proposed and closed SI : Composition of aiding vectors from IOs, Package, PCB.

➤ GPIO cell improvements

- **Usage of series termination in IO cell:** A common practice of using series termination on the output path to reduce drive while using margin for other optimizations to not go below minimum DC requirements.
- **MOS resistance to ZTCR ratio :** Reducing MOS resistance and increasing ZTCR factor in accounting for same total output resistance, thereby reducing variation over temperature. This helps reduce faster slews (di/dt).
- **Predrivers :** Degradation of predrivers to increase the slew of signal transitions, reducing di/dt .

➤ **Leadframe enhancements, Double bonding pads :** Widening of supply leadfingers, double bonding of pads to reduce L.

➤ **PCB Gnd :** Comprehension of PCB Gnd in package subckt to reduce loop inductances.

➤ **Board resistor :** External Res. on few high drive cells to reduce Ground bounces.

➤ **Customer usage :** Understanding broader customer usage with predecessor device and reduce the max. load cases and hence reduce max to min delay differences.

Results

Below table shows the overall SI aspects variation on design vectors and summarizes the solution strategy.

	Reliability	Noise margins		
#pins	VDDIO (Overshoot) at PAD	VIH(min)	VIL (Max)	Knob
N	< Lim	< Lim	~Lim	Previous design Reference (VDDIO + 5% tolerance)
60% of N	> Lim	< Lim	> Lim	Problem stat : Pin count reduction (40% reduction)
	>> Lim	~Lim	>> Lim	Problem stat : VDDIO + 10% tolerance (new SPEC requirement)
	~Lim	< Lim	> Lim	IO design opt (not sufficient)
	< Lim	< Lim	> Lim	IO design opt+wider leadwidth+Double bond (closer to limits)
	< Lim	< Lim	< Lim	+ PCB Gnd comprehension (Reached limits)

< Limits

Just around Limits

Crossed limits, few fixes reqd

Not acceptable values

Summary

- High performance microcontroller with power pins reduction of 40% plus increased supply tolerance - a challenging task dealt with solution on multiple design vectors has been achieved, used for our design.
- Enables us to support low-cost voltage regulator plus more functionality for customers – an important reach forward from competitive marketing standpoint.
- Industry available solutions have area impact, presented solutions are cost-effective i.e., without area increase of GPIO. Any small increase in GPIO area would have increased overall die-size.
- IO delay increase due to predriver degradation, higher values of series termination have been compensated with die level optimizations.
- Solution vectors show cohesive work from different domains – SOC, IO design, Package, PCB enabling higher signal to supply pin ratio.

Q & A